Youngjin (Luke) Kim

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Summary

PhD student in Electrical and Computer Engineering at USC specializing in EDA for advanced packaging. Experienced in GPU-accelerated EDA algorithm optimization, physical design for 2.5D/3D IC, and ML-driven design automation.

Education

University of Southern California (USC) — Los Angeles, CA
Ph.D. in Electrical and Computer Engineering — *Aug 2025 – Present*
- Selected Coursework: Hardware Foundations of ML, CAD of Digital Systems, Optimization for Information and Data Sciences

Yonsei University — Seoul, South Korea
B.S. in Electrical and Electronic Engineering — *Mar 2019 – Aug 2025*
- GPA: 3.83/4.0 (Major: 3.92/4.0)

Skills

Languages: C/C++ (libtorch, CUDA), Python (PyTorch), Verilog, Chisel, MATLAB, Shell Script
HW Tools: Keysight ADS, Cadence (Innovus, Virtuoso), Siemens (HyperLynx, Xpedition), Synopsys (DC, PrimeTime), Xilinx HLS
Tools: Git, Linux, Docker, LaTeX

Experience

Machine Learning Architecture Systems — PhD Intern — May 2026 – Aug 2026 (Incoming)
Keysight Technologies – Supervisor: Dr. Fabio Alessio Marino — *Calabasas, CA*
- Developing **autonomous neural architecture generation** and meta-learning frameworks in **C++/CUDA and libtorch**, targeting operator-learning model families (**GNNs, GNOs, FNOs**, and Transformer variants) for signal integrity applications
- Prototyping **architecture controllers** that adapt model topology, receptive fields, and operator depth based on real-time learning feedback for **resolution-invariant signal integrity ML architectures**

Graduate Research Assistant — Aug 2025 – Present
University of Southern California, SCCAD Lab – Advisor: Prof. Sung-Kyu Lim — *Los Angeles, CA*
- Building the **OpenEYE** framework, a **GPU-accelerated differentiable platform** for signal integrity analysis and optimization in 2.5D IC interconnects, with **custom CUDA-based physical solvers** implemented on the **TorchEDA** autograd backend

Intern, Controller Development — Sep 2024 – Jan 2025
Samsung Memory Division, Signal Processing Task Group — *Hwaseong, South Korea*
- Designed hardware-accelerated **graph-based vector search engine** for **SSD controller** targeting AI datacenter storage using C/C++-based HLS on FPGA, achieving **20× speedup** over CPU baseline across **1B+ data points**
- Architected **prefetching mechanisms** and scheduling algorithms for multiple **Graph IPs** with optimized memory access patterns and pipeline latency reduction

Projects

Photonic AI Accelerator | *High-Speed Circuits Lab, Advisor: Prof. Woo-Young Choi* — Aug 2023 – Aug 2024
- Led **FPGA prototyping** of digital control system for **Silicon Micro Ring Modulator**-based photonic AI accelerator
- Built Python-based physical modeling and matrix-based **thermal crosstalk cancellation**, improving CNN accuracy on MNIST from **70% to 90%**

RISC-V Processor & Accelerator IPs | *HAI Lab, Advisor: Prof. Jaeyong Chung* — Sep 2024 – Aug 2025
- Built **RISC-V processor** with **ISA extensions** and transparent protocol adapter framework enabling modular integration of hardware accelerators
- Optimized **memory access patterns** via **HLS**, extending Samsung's vector search architecture for large-scale data processing

Selected Publications

OpenEYE: A Differentiable Engine for Signal Integrity Analysis and Optimization in 2.5D IC Interconnects — 2026
- **Y. Kim**, M. G. Park, M. A. Dolatsara, and S. K. Lim. *Submitted to IEEE/ACM ICCAD*, 2026

Thermal Crosstalk Cancellation for Photonic Weight Banks in Optic Neural Networks — 2024
- **Y. Kim**, Y. Ji, and W.-Y. Choi. *Oral Presentation*, July 2024